Attorney Docket No. 10559-401001
Application No. 09/823,235
Amendment dated April 12, 2004
Reply to Office Action dated January 14, 2004

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

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1. (Currently amended) An apparatus comprising:

a cache of ~~traces, each trace~~ trace information including ~~information about~~ interdependent instructions ~~among~~ which interdependent instructions include at least an associated instruction and ~~data dependency exists, the interdependent instructions including~~ a criterion instruction that is part of a program sequence and which is data dependent on said associated instruction; and

a processor that associates first information from the associated instruction with said criterion instruction to form said trace information.

2. (Currently amended) The apparatus of claim 1 wherein the trace information comprises a directed acyclic graph.

3. (Currently amended) The apparatus of claim 1 wherein the trace information includes pointers to the interdependent instructions.

4. (Cancelled)



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5. (Original) The apparatus of claim 1 wherein the interdependent instructions include the criterion instruction and instructions preceding the criterion instruction in the program sequence.

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6. (Currently amended) The apparatus of claim 1 wherein the interdependent instructions are classified into subslice types, the trace information including a pointer to each subslice that is formed by each type of the interdependent instructions.

7. (Original) The apparatus of claim 6 wherein each subslice is stored as dependent pieces.

8. (Currently amended) The apparatus of claim 1 wherein the information includes a triggering condition of the trace information, the interdependent instructions of the trace being executed when the triggering condition is met.

9. (Original) The apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the



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program sequence, the triggering condition being based on evaluation of an architectural state.

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10. (Original) The apparatus of claim 8 wherein the triggering condition includes a triggering instruction in the program sequence, the triggering condition being based on evaluation of a micro-architectural state.

11. (Currently amended) The apparatus of claim 1 wherein the information further includes a confidence metric of the trace information that predicts the likelihood of producing a correct result from executing the trace.

12. (Currently amended) The apparatus of claim 11 wherein the confidence metric of the trace information indicates whether or not the trace should be replaced by a new trace storing information about different instructions.

13. (Currently amended) The apparatus of claim 11 wherein the confidence metric of the trace information indicates whether or not the trace should be rebuilt using new information about the criterion instruction that arrives at the trace cache.



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14. (Original) The apparatus of claim 11 further comprising a counter having a counter value that indicates the number of times the trace has been executed, the counter valuc, when exceeding a frequency threshold of the trace, triggering the trace to be rebuilt.

15. (Original) The apparatus of claim 1 wherein traces that are independent of each other and adjacent in the program sequence are grouped into a very-long-instruction-word for parallel executions.

16. (Original) The apparatus of claim 1 wherein traces that are data dependent of each other are chained together for serial executions.

17. (Currently amended) The apparatus of claim 1 further comprising an instruction pointer that indexes the trace information, the instruction pointer pointing to a first instruction or a last instruction of the interdependent instructions.



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18. (Original) The apparatus of claim 1 further comprising:

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a main pipeline executing the program sequence; and at least one secondary pipeline disjoint from the main pipeline executing the interdependent instructions.

19. (Original) The apparatus of claim 1 wherein the interdependent instructions are executed by a secondary thread on a pipeline, and the program sequence is executed by a main thread on the same pipeline.

20. (Currently amended) A method comprising:

identifying a criterion instruction incurring latency in a program sequence;

capturing the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion instruction being interdependent;

storing additional instructions relating to said criterion instruction; and

storing a trace in a trace cache, the trace including information about the criterion instruction interpreted



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according to said additional instructions and the preceding instructions.

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21. (Currently amended) The method of claim 20 wherein the information is in a form of a directed acyclic graph.

22. (Original) The method of claim 20 wherein the latency includes a long latency that exceeds a predetermined time threshold, a frequent latency that exceeds a predetermined recurrence threshold, or a long and uncertain latency that exceeds a mean threshold and a variance threshold.

23. (Original) The method of claim 20 further comprising dynamically identifying the criterion instruction based on information derived from previous executions.

24. (Original) The method of claim 20 further comprising capturing the criterion instruction and the preceding instructions by a buffer.

25. (Original) The method of claim 20 further comprising locating an existing trace in the trace cache before storing the



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trace, the existing trace and the trace to be stored having the same first instruction or the same last instruction.

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26. (Original) The method of claim 20 further comprising rebuilding the trace after a duration of time interval that grows each time the trace is rebuilt until the duration reaches a predetermined time limit.

27. (Original) The method of claim 20 further comprising storing, in an array, the information about the criterion instruction and the preceding instructions.

28. (Original) The method of claim 27 wherein the array further includes a subslice type for each of the instructions, the subslice type being a result of classifying the instructions.

29. (Currently amended) A computer program residing on a computer readable medium comprising instructions for causing a computer to:

identify a criterion instruction incurring latency in a program sequence;



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capture the criterion instruction and instructions preceding the criterion instruction in the program sequence, the preceding instructions and the criterion instruction being interdependent;

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storing additional instructions relating to said criterion instruction; and

store a trace in a trace file, the trace including information about the criterion instruction interpreted according to said additional instructions, the preceding instructions, and interdependency among the criterion instruction and the preceding instructions.

30. (Original) The computer program of claim 29 wherein an analysis window defined in the computer program causes the computer to capture the criterion instruction and preceding instructions.

31. (Original) The computer program of claim 29 wherein the computer identifies the criterion instruction by profiling the program sequence.



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Kindly add the following new claims.

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32. (New) The apparatus as in claim 1, wherein there are multiple associated instructions associated with said criterion instruction, and said processor forms first trace information using a first of said associated instructions, and second trace information using a second of said associated instructions.

33. (New) The apparatus as in claim 1, wherein said criterion instructions are instructions which represent relatively long latencies in execution.

34. (New) The apparatus as in claim 1, wherein the criterion instructions include template data for an instruction form, and the associated instructions include information that assigns values of register information within the criterion instructions.

35. (New) The method as in claim 20, further comprising associating multiple different associated instructions with said criterion instruction, and said storing comprising forms first trace information using a first of said associated instructions, and second trace information using a second of said associated instructions.



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36. (New) The method as in claim 20, wherein said criterion instructions are instructions which represent relatively long latencies in execution.

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37. (New) The method as in claim 20, wherein the criterion instructions include data for an instruction form, and said storing comprising associating information from said additional instructions as register information within the criterion instructions.

38. (New) A program as in claim 29, further comprising associating multiple different associated instructions with said criterion instruction, and said storing comprising forms first trace information using a first of said associated instructions, and second trace information using a second of said associated instructions.

39. (New) A program as in claim 29, wherein said criterion instructions are instructions which represent relatively long latencies in execution.



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40. (New) A program as in claim 29, wherein the criterion instructions include data for an instruction, and said storing comprising associating information from said additional information as values of register information within the criterion instructions.



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